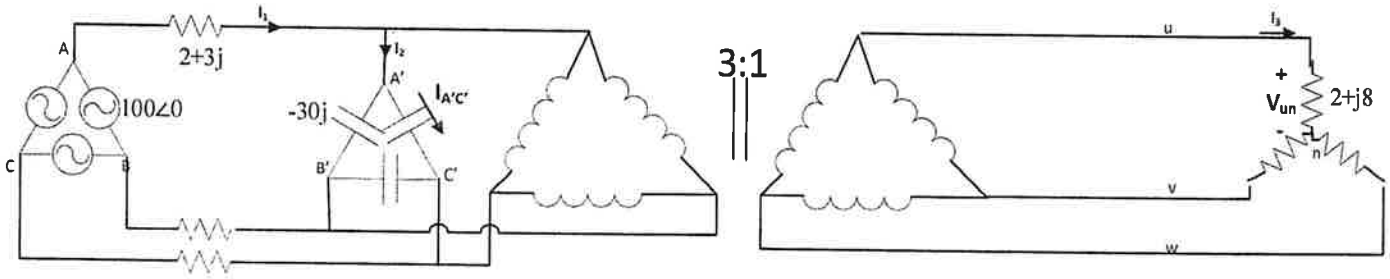
Problem : P6 **Area: `Communications/Signal Processing** **Student Code____**

For the IIR filter given by the difference equation $y[n]+y[n-1]-2y[n-3]=6x[n]-5x[n-3]$, calculate the transfer function H(z). You may assume all initial conditions are zero.

Problem: P14 **Area: Power** **Student Code: _____**

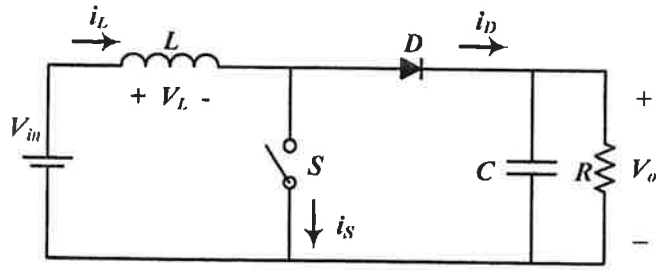
In the following circuit, find the following:

a) I_1, I_2, and I_3 (60 points).
b) $I_{A'C'}$ (Capacitor current) (10 points).
c) Phase voltage of the load (2+8j) equal to V_{un} (10 points).
d) 3-phase complex power of the source (20 points)



Problem: 15 **Area: Power** **Student Code:_____**

A Boost dc-dc converter has the following parameters: $V_{in} = 200$ V, $d = 0.25$, $V_{out} = 300$ V, $L = 100$ μH, and $f_{sw} = 100$ kHz.



a) Find the peak value of the inductor current.

b) Accurately plot the waveform of the inductor current.

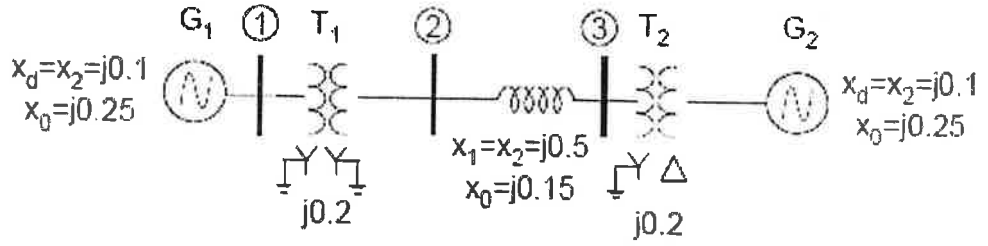
c) Find the average value of the inductor current.

d) Find the input power.

e) Find the value of the load resistor.

Problem: 16 **Area: Power** **Student Code:_____**

In the system shown below, a solid single line-ground fault occurs on bus 3. Both generators are solidly grounded.



The prefault voltages are 1.0 per unit. What are the positive, negative and zero sequence fault currents in line 2-3 during the fault?

Problem : 19 **Area: Waves & Devices** **Student Code:_____**

Constants*	Equations*
▪ Elementary charge = 1.6×10^{-19} [C] ▪ kT = 0.0259 [eV], kT/q = 0.0259 [V] (at 300 K) ▪ Intrinsic concentration = 10^{10} [cm^{-3}] (for silicon at 300 K)	▪ $n_o p_o = n_i^2$ ▪ $n_o = n_i \exp[(E_F - E_i) / kT]$ or $(E_F - E_i) = kT \ln(n_o/n_i)$ ▪ $p_o = n_i \exp[(E_i - E_F) / kT]$ or $(E_i - E_F) = kT \ln(p_o/n_i)$ ▪ $\sigma = q(n\mu_n + p\mu_p)$

* Definitions of parameters are not given; it is expected that the examinees interpret the meaning.

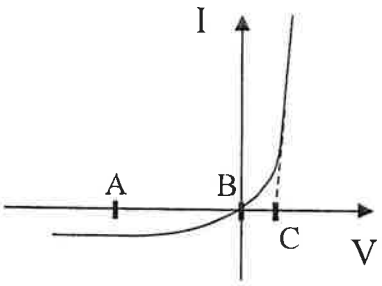
I. An abrupt silicon p-n junction has a net donor concentration of 10^{15} cm^{-3} in the n-side and an unknown acceptor concentration in the p-side, respectively. Answer the following questions assuming all dopants are ionized at room temperature (i.e. 300 K).

a. [25%] Calculate the carrier concentrations and fill out the following table.

	Majority carrier type (circle one)	Majority carrier concentration	Minority carrier type (circle one)	Minority carrier concentration
n-type	electron / hole	( ) [cm^{-3}]	electron / hole	( ) [cm^{-3}]

b. [25%] Calculate the contact (or built-in) voltage across the depletion region (or space charge region) at thermal equilibrium, when $(E_i - E_F)$ in the p-side is 0.45 eV: ( ) [V]

c. [20%] Fill out the following table based on the diode I-V characteristics shown below (I: diode current, V: external bias).



External bias V [V]	Voltage difference across the depletion region [V]
A. - 2.0	( )
B. 0.0	( )
C. 0.6	( )

II. [30%] Consider a silicon sample doped with donors (10^{14} cm^{-3}) at room temperature. Excess carriers by photon absorption (steady-state concentrations of 2.0×10^{13} cm^{-3} electrons and 2.0×10^{13} cm^{-3} holes) are generated during a light illumination. Calculate the increased conductivity (i.e. additional conductivity excluding the base conductivity without illumination) of the sample during illumination (electron mobility = 1,500 $cm^2/V \cdot sec$; hole mobility = 500 $cm^2/V \cdot sec$).

Problem: P21 **Area: Computational Intelligence** **Code #**_____

Answer the questions for parts **a** and **b** below.

(a) In developing an optimal multilayer perceptron with the back-propagation algorithm, describe the considerations for the network architecture, transfer functions, and number and type of network outputs.

(b) Describe the considerations for training, validating, and testing a multilayer perceptron with back-propagation algorithm for a 2 class dataset of 10,000 feature vectors with 8,000 feature vectors of class 1 and 2,000 feature vectors of class 2.

Problem: P22 **Area: Computational Intelligence** **Code #_____**

(a) What is Computational Intelligence (CI)?

(b) Describe the difference between the traditional Artificial Intelligence (AI) and the modern CI. Give an example of an application where AI is the more appropriate paradigm. Give an example of an application where CI is the more appropriate paradigm. Justify your application selections for AI and CI.

Problem: P24 **Area: Computational Intelligence** **Code #_____**

Answer the following questions.

(a) Describe the different types of hardware evolution. Provide diagrams where possible.

(b) Define the following terms:

(i) Explainable AI

(ii) Deep Learning

Problem : 25 **Area Computer architecture and Embedded Systems** **Student Code____**

Describe the unique aspects of Von Neumann and Harvard architectures. Which architecture is more advantageous for embedded systems that use a microcontroller and for embedded systems that use a general-purpose microprocessor? Explain your answer.

Problem : 26 **Area Computer architecture and Embedded Systems** **Student Code____**

Answer the questions for parts a-c below:

(a) Describe what is meant by an addressing mode for microprocessor architecture design. Describe the relationship between addressing modes and a microprocessor's instruction set.

(b) Describe three different addressing modes that are commonly used in microprocessor design.

(c) Which addressing mode is most appropriate for accessing elements of an array stored in internal data memory?

Problem : 27 **Area Computer architecture and Embedded Systems** **Student Code____**

Suppose you have two implementations of the same instruction set architecture. For some program which has 1 million instructions,

- Machine A has a clock cycle time of 100ps and an average CPI (Cycles Per Instruction) of 2.0.
- Machine B has a clock cycle time of 130ps and an average CPI of 1.5.

a) What machine is faster for this program, and by how much (calculate performance ratio, also known as speedup)?

b) If overclocking (i.e., driving the given machine with faster clock) of the slower machine is possible, what clock rate should be used to execute the given program to achieve the same execution time of the faster machine?

Problem: P29 **Area: Integrated Circuits and Logic Design** **Code #_____**

Find the minimal sum and the minimal products expressions using k-maps for the function: $f(w,x,y,z) = \prod(0,1,2,5,7,11,14,15) + dc(8,9)$. Note that dc refers to don't care terms.

Problem: P30 **Area: Integrated Circuits and Logic Design** **Code #_____**

Draw the 2-input NAND and 2-input NOR implementations for the logic expression $f = AB + \bar{A}C + B\bar{C}$

Problem: P31 **Area: Integrated Circuits and Logic Design** **Code #_____**

Answer the questions for parts **a** and **b** below.

a) Describe what a latch is and what a flip-flop is. Describe the differences between a latch and a flip-flop. Provide examples of real-world devices that use latches and flip-flops.

b) Describe the difference between a rising edge and a falling edge flip-flop. Illustrate the difference using a schematic/drawing.

Problem: P32 **Area: Integrated Circuits and Logic Design** **Code #**_____

State Machine Design Problem

Design a 3-bit counter with one control signal that works as follows

Control Inputs (CI) **A**	**Operation**
1	Down Counter 7,6,5,4,3,2,1,0,7,6,5,4,3,2,1,0,...
0	Counting Sequence 4,3,5,7,2,1,6,0,4,3,5,7,2,1,6,0,..

CI	Present State			Next State			Next State Inputs		
A	Q_2	Q_1	Q_0	Q_2^*	Q_1^*	Q_0^*	T_2	T_1	T_0
0	0	0	0						
0	0	0	1						
0	0	1	0						
0	0	1	1						
0	1	0	0						
0	1	0	1						
0	1	1	0						
0	1	1	1						
1	0	0	0						
1	0	0	1						
1	0	1	0						
1	0	1	1						
1	1	0	0						
1	1	0	1						
1	1	1	0						
1	1	1	1						

Complete the following:

- The state machine uses T Flip Flops as memory elements. Fill in the Next State and Next State Inputs columns in the partially filled table above.
- Based on the filled table, draw the state transition diagram.

Problem: P33 **Area: Networking, Security, and Dependability** **Student Code: ____**

This problem has two parts. For full credit, you must answer both parts correctly.

Consider a block cipher that uses 8-bit blocks and is based on the basic DES architecture (Feistel network), with two rounds and no initial or final permutation. The scrambling function for each round is defined as:

$$f_i(x) = (2i \cdot x \cdot K) \bmod 15, \qquad i = 1, 2, \quad \text{where } K = 7$$

Answer the following questions and show your work.

a. If the plaintext is 00101001, what is the ciphertext?

b. Draw the Feistel cipher network.

Problem: P35 Area: Networking, Security, and Dependability **Student Code: ____**

This problem has two parts. For full credit, you must answer both parts correctly.

a. Suppose a router has built up the routing table shown in the table below. The router can deliver packets directly over interfaces 0 or 1, or it can forward packets to routers R2, R3, or R4. Assume the router uses the longest prefix match. Determine the next hop for a packet addressed to each of the destinations (i, ii, and iii) listed below the table. Note that the destination addresses, subnet numbers, and subnet masks are in hex rather than dotted decimal notation. Show your work.

SubnetNumber	SubnetMask	NextHop
80.60.AA.00	FF.FF.FE.00	Interface 0
80.60.A8.00	FF.FF.FE.00	Interface 1
80.60.A6.00	FF.FF.FE.00	R2
80.60.A4.00	FF.FF.FC.00	R3
default		R4

i. 80.60.A7.97

ii. 80.60.A5.79

iii. 80.60.A3.97

b. Suppose hosts A and B are on an Ethernet LAN with IP network address 200.0.0/24. It is desired to attach a host C to the network via a direct connection to B, as shown in the figure below. Answer both parts below. Show your work.

i. Explain how to do this with subnets; give sample subnet assignments.

ii. Assume that an additional network prefix is not available. What does this do to the size of the Ethernet LAN?